PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
STEPHENS S. FORD
STOLOWITZ FORD COWGER LLP
621 SW MORRISON STREET, SUITE 600
PORTLAND, OREGON 97205

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	22 JUL 2009
Applicant's or agent's file reference 5869-0102	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 09/38126	24 March 2009 (24.03.2009)	24 March 2008 (24.03.2008)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H04M 1/00 (2009.01)
USPC - 379/392.01

Applicant MATECH, INC.

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	05 July 2009 (05.07.2009)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 09/38126

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing

      ☐ contained in the international application as filed

      ☐ filed together with the international application in electronic form

      ☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 09/38126

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1 - 13	YES
	Claims	None.	NO
Inventive step (IS)	Claims	1 - 9	YES
	Claims	10 - 13	NO
Industrial applicability (IA)	Claims	1 - 13	YES
	Claims	None.	NO

2. Citations and explanations:

Claims 10 - 13 lack an inventive step under PCT Article 33(3) as being obvious over US 2007/0133442 A1 to Masuda et al. (hereinafter 'Masuda'), in view of US 2003/0185403 A1 (Sibbald).

Regarding claim 10, Masuda teaches an audio circuit (abstract, para. [0048]), comprising: an analog circuit including a differential output amplifier (para. [0045]), an differential input amplifier (para. [0045]), and a bridge circuit coupled between the differential output amplifier and the differential input amplifier (para. [0040], Fig. 1); and a digital signal processing circuit configured to generate one or more first set of signal filter coefficients from a first signal input into the analog circuit and generate one or more second set of filter coefficients from a second signal output from the analog circuit (claim - 2, 3). Masuda does not teach the digital signal processing circuit generating an transfer function from the first and second set of filter coefficients and generating an output signal from the transfer function that is applied to the second signal output from the analog circuit. However Sibbald teaches a method of improving the audibility of sound from a loudspeaker (abstract), wherein the method includes a digital signal processing circuit generating an transfer function from the first and second set of filter coefficients and generating an output signal from the transfer function that is applied to the second signal output from the analog circuit (para. [0010], [0035]). It would have been obvious to one skilled in the art to combine the teachings of Masuda with those of Sibbald in order to reduce the amount of noise in the audio signal.

Regarding claim 11, Masuda teaches an D/A converter DAC coupling the first signal input to the differential output amplifier via a first high pass filter (corrective filter, para. [0117]); and a A/D converter (ADC) coupling the second signal output from the analog circuit to a second high pass filter in the digital signal processing circuit (para. [0031], [0032]).

Regarding claim 12, Masuda teaches that the second set of filter coefficients are associated with a transfer function for a signal pathway from the DAC, through the analog circuit and ADC, and to the second high pass filter (corrective filter, para. [0117]; claim - 2, 3).

Regarding claim 13, Masuda teaches a subtracter that subtracts the output signal from the transfer function from the second signal after the second signal passes through the second high pass filter to extract a transmission signal generated in the second signal by a transducer in the analog circuit (para. [0047], [0063]).

---(continued on Supplemental Pages)---

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

V.2. Citations and explanations:

Claims 1 - 9 meet the criteria set out in PCT Article 33(2)-(3).

Regarding claim 1, Masuda teaches a single-transducer full duplex circuit (para. [0022]), comprising: connecting terminals for connecting to an external digital circuit including an input terminal (DIN) into which a digital reception input signal is input, an output terminal (DoUT) into which a digital transmission output signal is output, and a learning activation input terminal (ILN) (abstract, Fig. 1); an analog signal processing circuit including: an analog differential output amplifier (ADO) which amplifies the output from a D/A converter (DAC); a bridge circuit consisting of first, second, and third resistors (RI, R2, and R3) and a single transducer (ZT) which are driven by an output of the analog differential output amplifier (ADO) (Fig. 1).

Neither Masuda nor the Prior art teach or fairly suggest an analog differential input amplifier (Am) which amplifies an equilibrium signal output by the bridge circuit, wherein an analog output signal of the analog differential input amplifier (Am) is supplied to an AID converter (ADC) ; a digital signal processing circuit including: a signal generator (SG); a first high pass filter (HPFI) into which the digital reception input signal is input through the input terminal (DIN) ; a first multiplier (MULI) which multiplies the output of the high pass filter (HPFI) by a reception volume coefficient (RRXv) ; a second multiplier (MUL2) which multiplies the input from the signal generator (SG) by a signal volume coefficient register (RsGv) an adder (ADD) which adds the output of the first multiplier (MULI) and the output of the second multiplier (MUL2), wherein the output of the adder (ADD) is supplied to the D/A converter (DAC) which converts it into an analog signal; a first signal delayer and power calculator (DLI) which delays the output signal of the adder (ADD) and calculates a first moving average power value (PWI) ; a second signal delayer and power calculator (DL2) which delays the output of the first signal delayer and power calculator (DLI) and calculates a second moving average power value (PW2) ; a delayed signal memory (XA[k]) which sequentially stores the output of the second signal delayer and power calculator (DL2) ; a transfer function identification filter (FILm) into which the output of the delayed signal memory (XA[k]) is input; a first filter coefficient memory (HA[k]) which stores a filter coefficient corresponding to the transfer function identification filter (FILm); a second high pass filter (HPF2) into which an output of the AID converter (ADC) is input; a fourth signal delayer (DL4) into which an output of the second high pass filter (HPF2) is input; a subtracter (SUB) which subtracts an output of the transfer function identification filter (FILm) from an output of the fourth signal delayer (DL4); a fourth multiplier (MUL4) which multiplies an output of the subtracter (SUB) by a transmission volume coefficient (RTXV); a third signal delayer and power calculator (DL3) which delays an output of the fourth multiplier (MUL4) and calculates a third moving average power value (PW3); an equalization filter (FILEQ) into which an output of the third signal delayer and power calculator (DL3) is input; and a second filter coefficient memory which stores a filter coefficient (HEQ[k]) of the equalization filter (FILEQ), wherein the transmission output terminal (DOUT) is driven by a digital transmission output signal output from the equalization filter (FILEQ) and the first filter coefficient (HA[k]) corresponding to the transfer function identification filter FILm identifies the transfer function from the input end of the D/A converter (DAC) to the output end of the second high pass filter (HPF2) via the analog signal processing circuit.

Claims 2 - 9 depend either directly or indirectly from claim, and therefore meet the criteria set out in PCT Article 33(2)-(3).

Claims 1 - 13 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.